

ABSTRACT

The circuit includes a delay circuit 1 for phase-
delaying clocks output from a voltage controlled
oscillator by a predetermined phase, a flip flop 2 for
capturing the clock delayed by the delay circuit at a
falling edge or rising edge of the data signal, an average
value circuit 3 for detecting a time average value of an
output of the flip flop, and a comparator 4 for comparing
in amplitude the time average value with a predetermined
fixed value and then issuing an alarm when out-of-sync of
a clock is detected.